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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/566,984	09/21/2006	Lay-lay Chua	Q93039	2855
23373	7590	04/10/2009	EXAMINER	
SUGHRUE MION, PLLC			JEFFERSON, QUOVAUNDA	
2100 PENNSYLVANIA AVENUE, N.W.				
SUITE 800			ART UNIT	PAPER NUMBER
WASHINGTON, DC 20037			2823	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/566,984	CHUA ET AL.	
	Examiner	Art Unit	
	QUOVAUNDA JEFFERSON	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 04 March 2009.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-25 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) 4-6 and 23-25 is/are allowed.
 6) Claim(s) 1-3 and 7-22 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____ .
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)	5) <input type="checkbox"/> Notice of Informal Patent Application
Paper No(s)/Mail Date _____.	6) <input type="checkbox"/> Other: _____ .

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 7-10, 18, and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by WIPO document WO 99/13692, issued by Cambridge Display Technology Limited (herein referred to as “Cambridge”).

Regarding claim 1, Cambridge teaches a method of making a transistor having first and second electrodes, a semiconductive layer, and a dielectric layer, said semiconductive layer comprising a semiconductive polymer and said dielectric layer comprising an insulating polymer; characterized in that said method comprises the steps of (i) depositing on the first electrode 4 a layer of a solution, said solution comprising material for forming the semiconductive layer (a polyanion/polycation solution that forms a bi-layer with the chemical compound that is shown in figures 2c and 2d), and material for forming the dielectric layer (a polyanion/polycation solution that forms a bi-layer with the chemical compound that is shown in figures 2a and 2b),

and (ii) optionally curing the layer deposited in step (i), wherein, in step (i), the solvent drying time, the temperature of the first electrode and the weight ratio of (material for forming the dielectric layer): (material for forming the semiconductive layer) in the solution are selected so that the material for forming the semiconductive layer and the material for forming the dielectric layer phase separate by self- organization to form an interface between the material for forming the semiconductive layer and the material for forming the dielectric layer (page 2, last paragraph, Page 5, line 25 to page 6, line 6, page 9, lines 7-27, and page 20, lines 3-25).

Regarding claim 7, Cambridge teaches the material for forming the semiconductive layer and the material for forming the dielectric layer comprises a diblock polymer (figure 2), said polymer comprising a semiconductive block (figures 2c and 2d) for forming the semiconductive layer and a dielectric block for forming the dielectric layer (figures 2a and 2b).

Regarding claim 8, Cambridge teaches the material for forming the semiconductive layer comprises one or more aromatic or heteroaromatic structural units (figure 2d).

Regarding claim 9, Cambridge teaches the one or more aromatic or heteroaromatic units independently are selected from the group consisting of

fluorenediyil, phenylene, phenylene vinylene, triarylamine, thiophenediyil, thiophene, oxadiazole and benzothiadiazole (figure 2d).

Regarding claim 10, Cambridge teaches the material for forming the dielectric layer comprises crosslinkable groups (figures 2a and 2b).

Regarding claim 18, Cambridge teaches the thickness of the dielectric layer is below 400 nm (page 6, lines 15-16).

Regarding claim 19, Cambridge teaches the thickness of the semiconductive layer is in the range of 10nm to 300nm (page 6, lines 15-16).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 2, 3, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over WIPO document WO 99/13692, issued by Cambridge Display Technology Limited (herein referred to as “Cambridge”).

Regarding claim 2, Cambridge fails to teach the weight ratio of (material for forming the dielectric layer): (material for forming the semiconductive layer) is in the range of from 0.5 to 2.

However, given the teaching of the references, it would have been obvious to determine the optimum thickness, temperature as well as condition of delivery of the layers involved See In re Aller, Lacey, and Hall (10 USPQ 2d 3-237) "It is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of either the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Any differences in the claimed invention and the prior art may be expected to result in some differences in properties. The issue is whether the properties differ to such an extent that the difference is really unexpected. In re Merck & Co., 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Appellants have the burden of explaining the data in any declaration they proffer as evidence of non-obviousness. Ex parte Ishizaka, 24 USPQ2d 1621, 1624 (Bd. Pat. App. & Inter. 1992).

An Affidavit or declaration under 37 CFR 1.132 must compare the claimed subject matter with the closest prior art to be effective to rebut a prima facie case of obviousness. In re Burckel, 592 F.2d 1175, 201 USPQ 67 (CCPA 1979).

Regarding claim 3, Cambridge fails to teach the solvent drying time is in the range of from 0.1 to 100s.

However, given the teaching of the references, it would have been obvious to determine the optimum thickness, temperature as well as condition of delivery of the layers involved See In re Aller, Lacey, and Hall (10 USPQ 23 3-237) "It is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of either the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that those chosen dimensions are critical. In re Woodruff, 919 f.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Any differences in the claimed invention and the prior art may be expected to result in some differences in properties. The issue is whether the properties differ to such an extent that the difference is really unexpected. In re Merck & Co., 800 F.2d 1091,231 USPQ 375 (Fed. Cir. 1986). Appellants have the burden of explaining the

data in any declaration they proffer as evidence of non-obviousness. Ex parte Ishizaka, 24 USPQ2d 1621, 1624 (Bd. Pat. App. & Inter. 1992).

An Affidavit or declaration under 37 CFR 1.132 must compare the claimed subject matter with the closest prior art to be effective to rebut a prima facie case of obviousness. In re Burckel, 592 F.2d 1175, 201 USPQ 67 (CCPA 1979).

Regarding claim 13, Cambridge fails to teach the material for forming the dielectric layer has a surface tension in the range of from 15 to 35 dyn/cm.

However, given the teaching of the references, it would have been obvious to determine the optimum thickness, temperature as well as condition of delivery of the layers involved. See In re Aller, Lacey, and Hall (10 USPQ 2d 3-237) "It is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of either the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 f.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Any differences in the claimed invention and the prior art may be expected to result in some differences in properties. The issue is whether the properties differ to

such an extent that the difference is really unexpected. In re Merck & Co., 800 F.2d 1091,231 USPQ 375 (Fed. Cir. 1986). Appellants have the burden of explaining the data in any declaration they proffer as evidence of non-obviousness. Ex parte Ishizaka, 24 USPQ2d 1621, 1624 (Bd. Pat. App. & Inter. 1992).

An Affidavit or declaration under 37 CFR 1.132 must compare the claimed subject matter with the closest prior art to be effective to rebut a prima facie case of obviousness. In re Burckel, 592 F.2d 1175, 201 USPQ 67 (CCPA 1979).

Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cambridge as applied to claims above, and further in view of Marks et al, US Patent 5,834,100.

Regarding claim 11, Cambridge fails to teach the material for forming the dielectric layer comprises one or more units having a low cohesive-energy density

Marks teaches the material for forming the dielectric layer comprises one or more units having a low cohesive-energy density (abstract) by teaching the use of siloxane as an appropriate material for an OLED device to provide an environmentally stable material over prolonged use of the device over a period of time.

It would be obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Cambridge with that of Marks because the use of siloxane as an appropriate material for an OLED device to provide an environmentally stable material over prolonged use of the device over a period of time.

Regarding claim 12, Marks teaches the one or more units having a low cohesive-energy density are selected from the group consisting of siloxane, perfluoroalkyl, perfluoroarylene ether, perfluoroalkylene ether (abstract).

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cambridge as applied to claims above, and further in view of Cheng et al, US Patent 6,737,303.

Regarding claim 14, Cambridge fails to teach the transistor is in top-gate configuration.

Cheng teaches the transistor is in top-gate configuration (figure 3) which is another alternative type of semiconductor device with a polymer layer that may be formed using a self-assembling process to form said polymer layer for a top-gate transistor.

It would be obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Cheng with that of Cambridge because it would

enable the practitioners of Cambridge another alternative type of semiconductor device with a polymer layer that may be formed using a self-assembling process to form said polymer layer for a top-gate transistor.

Claims 15-17, 20, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cambridge as applied to claims above, and further in view of Dimitrakopoulos et al, US Patent 5,981,970.

Regarding claim 15, Cambridge fails to teach the transistor is in bottom-gate configuration.

Dimitrakopoulos teaches the transistor is in bottom-gate configuration (figure 6) as an alternative type of semiconductor device which also uses a self-assembling layer to form a polymer material for a bottom-gate semiconductor device.

It would be obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Dimitrakopoulos with that of Cambridge because it would enable the practitioners of Cambridge an alternative type of device that could be made using the self-assembling layers of polymers.

Regarding claim 16, Cambridge teaches the material for forming the dielectric layer comprises one or more units having high affinity for the first electrode (page 14, lines 7-9)

Regarding claim 17, Cambridge teaches the first electrode is surface treated prior to step (i) with a material containing one or more units having high affinity for the first electrode page 14, lines 7-9).

Regarding claim 20, Cambridge fails to teach the transistor is a field-effect transistor.

Dimitrakopoulos teaches the transistor is a field-effect transistor (figure 6) as an alternative type of semiconductor device which also uses a self-assembling layer to form a polymer material for a bottom-gate semiconductor device.

It would be obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Dimitrakopoulos with that of Cambridge because it would enable the practitioners of Cambridge an alternative type of device that could be made using the self-assembling layers of polymers.

Regarding claim 22, Cambridge fails to teach a transistor obtainable by the method as defined in claim 1.

Dimitrakopoulos teaches a transistor obtainable by the method as defined in claim 1 (figure 6) as an alternative type of semiconductor device which also uses a self-assembling layer to form a polymer material for a bottom-gate semiconductor device.

It would be obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Dimitrakopoulos with that of Cambridge because it would enable the practitioners of Cambridge an alternative type of device that could be made using the self-assembling layers of polymers.

Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cambridge as applied to claims above, and further in view of Narayan, US Patent Application 2002/0084504.

Regarding claim 21, Cambridge fails to teach the transistor is a phototransistor.

Narayan teaches the transistor is a phototransistor (figure 1B), which is another alternative type of semiconductor device with a polymer layer that may be formed using a self-assembling process to form said polymer layer

It would be obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Narayan with that of Cambridge because it

would enable the practitioners of Cambridge another alternative type of semiconductor device with a polymer layer that may be formed using a self-assembling process to form said polymer layer

Allowable Subject Matter

Claims 4-6 and 23-25 are allowed. The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 4, prior art fails to teach a method of making a transistor having first and second electrodes, a semiconductive layer, and a dielectric layer; said semiconductive layer comprising a semiconductive polymer and said dielectric layer comprising an insulating polymer; characterized in that said method comprises the steps of (i) depositing on the first electrode a layer of a solution, said solution comprising material for forming the semiconductive layer and material for forming the dielectric layer, wherein the material for forming the dielectric layer is mixed with the material for forming the semiconductive layer in the solution. Claims 5, 6, and 23-25 are dependent upon claim 4 and are therefore allowable.

Response to Arguments

Applicant's arguments, see After Final Reconsideration, filed March 4, 2009, with respect to the rejection(s) of claim(s) 1-25 under USC 102(e) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of cited prior art, as stated above, for claims 1-3 and 7-22.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to QUOVAUNDA JEFFERSON whose telephone number is (571)272-5051. The examiner can normally be reached on Monday thru Friday 7AM-3:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Michelle Estrada/
Primary Examiner, Art Unit 2823

QVJ